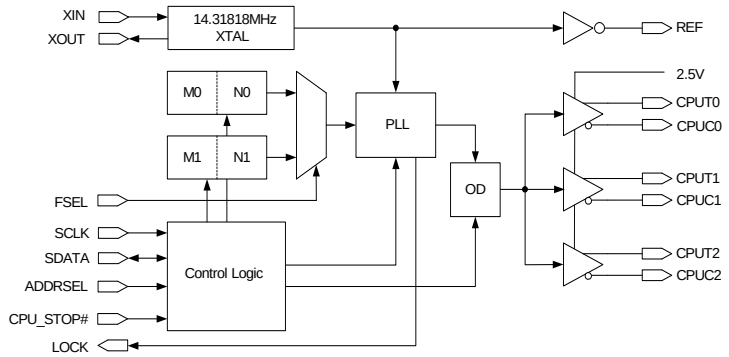
# CY28508

## 333 MHz Low-Voltage Differential SSCG

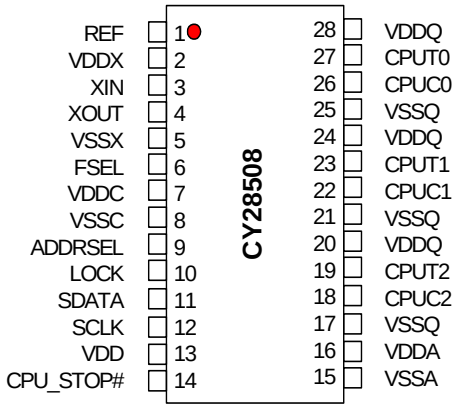
### Features

- Supports HSTL-compatible differential outputs using recommended termination scheme
- Three differential pairs of clocks
- From 112.5 MHz to 225.0 MHz and from 166.6 MHz to 333.3-MHz output frequency
- One REF 14.318 MHz clock
- Dual Dial-a-Frequency® programmable registers
- Smooth-Track™ frequency target slew rates as low as 100 KHz/usec in /2 mode and 70 KHz/usec in /3 mode
- Cypress Spread Spectrum for best electromagnetic interference (EMI) reduction
- Four center-spread settings
- $I^2C$ register programmable options
- Two selectable $I^2C$ addresses
- Block and byte mode $I^2C$ operation
- 3.3V core operation
- 2.5V output operation
- 28-pin SSOP package

### Block Diagram




### Pin Configuration



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## Pin Description [1]

| Pin | Name | Type | Power | Description |
|---|---|---|---|---|
| 1 | REF | O | VDDX | **Reference Clock**. 3.3V 14.318-Mz clock output. |
| 3 | XIN | I | VDDX | **Crystal Connection or External Reference Frequency Input**. This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input. |
| 4 | XOUT | O | VDDX | **Crystal Connection**. Connection for an external 14.318-MHz crystal output. |
| 27, 23, 19 | CPUT[0:2] | O | VDDQ | **CPUT Clock Outputs**: Differential True CPU clock outputs. |
| 26, 22, 18 | CPUC[0:2] | O | VDDQ | **CPUC Clock Outputs**: Differential Complementary CPU clock outputs. |
| 6 | FSEL | I, PU 250KΩ | VDD | **3.3V LVTTL input for CPU frequency selection**. 0 = M&N register set 0, 1 = M&N register set 1. |
| 11 | SDATA | I/O | VDD | **$I^2C$-compatible SDATA**. |
| 12 | SCLK | I | VDD | **$I^2C$-compatible SCLOCK**. |
| 14 | CPU_STOP# | I, PU 250KΩ | VDD | **CPU stop**. 1 = CPUT/C running, 0 = CPUT stopped synchronously low and CPUC stopped synchronously high. REF remains running. |
| 9 | ADDRSEL | I, PD 250KΩ | VDD | **$I^2C$ address selection**. 0 = D2, 1 = D4. |
| 10 | LOCK | Open Drain | VDD | **It is recommended that an external 10KΩ resistor is connected to this pin**. With this resistor, 1 = Signifies the VCO has locked onto the target frequency. 0 = Not locked to the designated M&N register pair target frequency. |
| 16 | VDDA | PWR | | **3.3V power supply for analog PLL**. |
| 15 | VSSA | GND | | **Ground for analog PLL**. |
| 28, 24, 20 | VDDQ | PWR | | **2.5V power supply for output buffers**. |
| 25, 21, 17 | VSSQ | GND | | **Ground for output buffers**. |
| 2 | VDDX | PWR | | **3.3V power supply for oscillator**. |
| 5 | VSSX | GND | | **Ground for oscillator**. |
| 7 | VDDC | PWR | | **3.3V power supply for core**. |
| 8 | VSSC | GND | | **Ground for core**. |
| 13 | VDD | PWR | | **3.3V power supply**. |

## Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*. The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The Byte Count value returned is 09h.

The slave receiver address is either D2 or D4, depending on the state of the ADDRSEL pin.

**Note:**
1. Throughout this document logic 0 and logic 1 state signals are referenced. As a clarification it should be understood that 1 = high and 0 = low voltage levels. These levels are defined in the DC Electrical Specifications of this data sheet.

**Table 1. Command Code Definition**

| Bit | Description |
|---|---|
| 7 | 0 = Block read or block write operation<br>1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be ‘0000000’ |

**Table 2. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits<br>‘00000000’ stands for block operation | 11:18 | Command Code – 8 bits<br>‘00000000’ stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29:36 | Data byte 0 from master – 8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 1 from master – 8 bits | 30:37 | Byte count from slave – 8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| .... | Data bytes from master/Acknowledge | 39:46 | Data byte 0 from slave – 8 bits |
| .... | Data Byte N – 8 bits | 47 | Acknowledge |
| .... | Acknowledge from slave | 48:55 | Data byte 1 from slave – 8 bits |
| .... | Stop | 56 | Acknowledge |
| | | .... | Data bytes from slave/Acknowledge |
| | | .... | Data byte N from slave – 8 bits |
| | | .... | Not Acknowledge |
| | | .... | Stop |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address – 7 bits | 2:8 | Slave address – 7 bits |
| 9 | Write = 0 | 9 | Write = 0 |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code – 8 bits<br>‘1xxxxxxx’ stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed | 11:18 | Command Code – 8 bits<br>‘1xxxxxxx’ stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte from master – 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address – 7 bits |
| 29 | Stop | 28 | Read = 1 |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave – 8 bits |
| | | 38 | Not Acknowledge |
| | | 39 | Stop |

## Serial Control Registers

### Byte 0 : CPU Control Register

| Bit | @Pup | Name | Description |
|---|---|---|---|
| 7 | HW | LOCK | Lock Detect: 0 = not at final frequency, 1 = VCO locked (read-only). |
| 6 | 0 | SS_ENABLE | 0 = disabled, 1 = enabled. |
| 5 | 0 | SST1 | Select spread percentage 1. See *Table 4* |
| 4 | 1 | SST0 | Select spread percentage 0. See *Table 4* |
| 3 | 1 | REF | REF Output Enable<br>0 = Disabled (three-stated)), 1 = Enabled |
| 2 | 1 | CPUT/C2 | CPU2 Output Enable<br>0 = Disabled (three-stated), 1 = Enabled |
| 1 | 1 | CPUT/C1 | CPU1 Output Enable<br>0 = Disabled (three-stated), 1 = Enabled |
| 0 | 1 | CPUT/C0 | CPU0 Output Enable<br>0 = Disabled (three-stated), 1 = Enabled |

**Table 4. Spread Spectrum Table**

| SST1 | SST0 | % Spread |
|---|---|---|
| 0 | 0 | ±0.125% Center spread Lexmark™ profile |
| 0 | 1 | ±0.25% Center spread Lexmark profile |
| 1 | 0 | ±0.5% Center spread Lexmark profile |
| 1 | 1 | ±0.5% Center spread Linear profile |

Glitch-free operation for both enabling and disabling Spread Spectrum. To achieve down spread operation, reprogram the N register to drop the frequency by half the spread amount.

### Byte 1: Dial-a-Frequency Control Register N0 [default = 112.35 MHz, N = 43d, ODSEL = 1]

| Bit | @Pup | Description |
|---|---|---|
| 7 | 0 | Test Mode: 0 = normal operation, 1 = phase-locked loop (PLL) bypass mode, when OD = 3 then /3, when OD = 2 then /2. |
| 6 | 0 | N6, most significant bit (MSB). |
| 5 | 1 | N5 |
| 4 | 0 | N4 |
| 3 | 1 | N3 |
| 2 | 0 | N2 |
| 1 | 1 | N1 |
| 0 | 1 | N0, least significant bit (LSB). |

### Byte 2: Dial-a-Frequency Control Register M0 [default = 112.35MHz, M = 49d, ODSEL = 1]

| Bit | @Pup | Description |
|---|---|---|
| 7 | 0 | The charge pump current value during Smooth-Track can be programmed to normal mode (2xICP) by setting this bit to “1.” The default value of “0” (1xICP) will program the charge pump current to half of normal and will reduce the bandwidth and hence the slew rate. |
| 6 | Pin 6 | FSEL operational status, whether HW or SW. 0 = M&N0, 1 = M&N1 (read only). |
| 5 | 1 | M5 MSB |
| 4 | 1 | M4 |
| 3 | 0 | M3 |
| 2 | 0 | M2 |
| 1 | 0 | M1 |
| 0 | 1 | M0, LSB |

**Byte 3: Dial-a-Frequency Control Register N1 [default = 224.70 MHz, N = 86d, ODSEL = 1]**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 0 | Reserved, set = 0. |
| 6 | 1 | N6, MSB |
| 5 | 0 | N5 |
| 4 | 1 | N4 |
| 3 | 0 | N3 |
| 2 | 1 | N2 |
| 1 | 1 | N1 |
| 0 | 0 | N0, LSB |

**Byte 4: Dial-a-Frequency Control Register M1 [default = 224.70 MHz, M = 49d, ODSEL = 1]**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 1 | Reserved, set = 1. |
| 6 | 1 | SWODSEL: Output divider select. 0 = /2, 1 = /3.<br>**Changing the output divider causes large instantaneous changes in the CPU pulse width and should only be changed before system operation is to occur**. |
| 5 | 1 | M5 MSB. |
| 4 | 1 | M4 |
| 3 | 0 | M3 |
| 2 | 0 | M2 |
| 1 | 0 | M1 |
| 0 | 1 | M0, LSB. |

**Byte 5: Dial-a-Frequency Control Register N2 – Only Bit 7 is Used by the CY28508**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 0 | UP/DN pulse width limit. During Smooth-Track, the bandwidth hence the slew rate is controlled through limiting the pulse width of the UP/DN pulse outputs of the phase detector going to the charge pump. The default is 0 = 20 ns and can be programmed to 1 = 40 ns, which will increase the slew rate. |
| 6 | 0 | Reserved, set = 0. |
| 5 | 1 | Reserved, set = 1. |
| 4 | 1 | Reserved, set = 1. |
| 3 | 0 | Reserved, set = 0. |
| 2 | 0 | Reserved, set = 0. |
| 1 | 0 | Reserved, set = 0. |
| 0 | 0 | Reserved, set = 0. |

**Byte 6: Dial-a-Frequency Control Register M2 – Only Bits 6 and 7 are Used by the CY28508**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 1 | FSEL Control: 1 = HW FSEL, 0 = SW FSEL |
| 6 | 1 | SW FSEL: 0 = SW MN0 select, 1 = SW MN1 select. Only valid when B6b7 = 0. |
| 5 | 1 | Reserved, set = 1. |
| 4 | 1 | Reserved, set = 1. |
| 3 | 0 | Reserved, set = 0. |
| 2 | 0 | Reserved, set = 0. |
| 1 | 0 | Reserved, set = 0. |
| 0 | 0 | Reserved, set = 0. |

**Byte 7: Dial-a-Frequency Control Register N3 - Only bit 7 is used by the CY28508**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 1 | Ns Setting. Ns is the total step time index during Smooth-Track for each increment or decrement during Smooth-Track. The default is 1 = 2048 and if you program a 0 = 1024, the step time will be half of this value. |
| 6 | 1 | Reserved, set = 0. |
| 5 | 0 | Reserved, set = 1. |
| 4 | 0 | Reserved, set = 1. |
| 3 | 0 | Reserved, set = 0. |
| 2 | 0 | Reserved, set = 0. |
| 1 | 0 | Reserved, set = 0. |
| 0 | 0 | Reserved, set = 0. |

**Byte 8: Dial-a-Frequency Control Register M3, Only bit 7 is used by the CY28508**

| Bit | @Pup | Description |
|---|---|---|
| 7 | 1 | ICP Tracking. In the default mode (= 1) the ICP current increases and the VCO frequency increase to maintain constant bandwidth. If you program a “0,” then the ICP current will stay constant. |
| 6 | 0 | Reserved, set = 0. |
| 5 | 1 | Reserved, set = 1. |
| 4 | 1 | Reserved, set = 1. |
| 3 | 0 | Reserved, set = 0. |
| 2 | 0 | Reserved, set = 0. |
| 1 | 0 | Reserved, set = 0. |
| 0 | 0 | Reserved, set = 0. |

## Dial-a-Frequency Feature

Dial-a-frequency gives the designer direct access to the reference divider (M) and the feedback divider (N) of the internal PLL.

VCO = (XTAL x 26.823) x (N/ M).

Output Frequency = VCO/Output Divider.

The VCO operating range is between 333 MHz and 675 MHz.

The user must not program N and M values that would result in a VCO frequency outside of this specified range.

## Hardware Switching of Dial-a-Frequency Registers

The architectural design of the HW Smooth-Track feature allows the system designer to configure two DAF registers that are selected via an FSEL input pin to select the desired final frequency. This slew rate control is defined as Smooth-Track and is used for all frequency change values programmed into the two DAF registers. There exists a LOCK output signal, which will activate when the final frequency is achieved by the VCO. For Ns = 2048 and M = 48, each step takes 492 µs such that to increment 40 steps would take 19.7 ms.

Spread Spectrum Modulation Rate

Fmodulation (KHz) = 1500.25/M.

The profile of the modulation is tuned for M = 48, such that deviations from this value could affect the Lexmark profile.

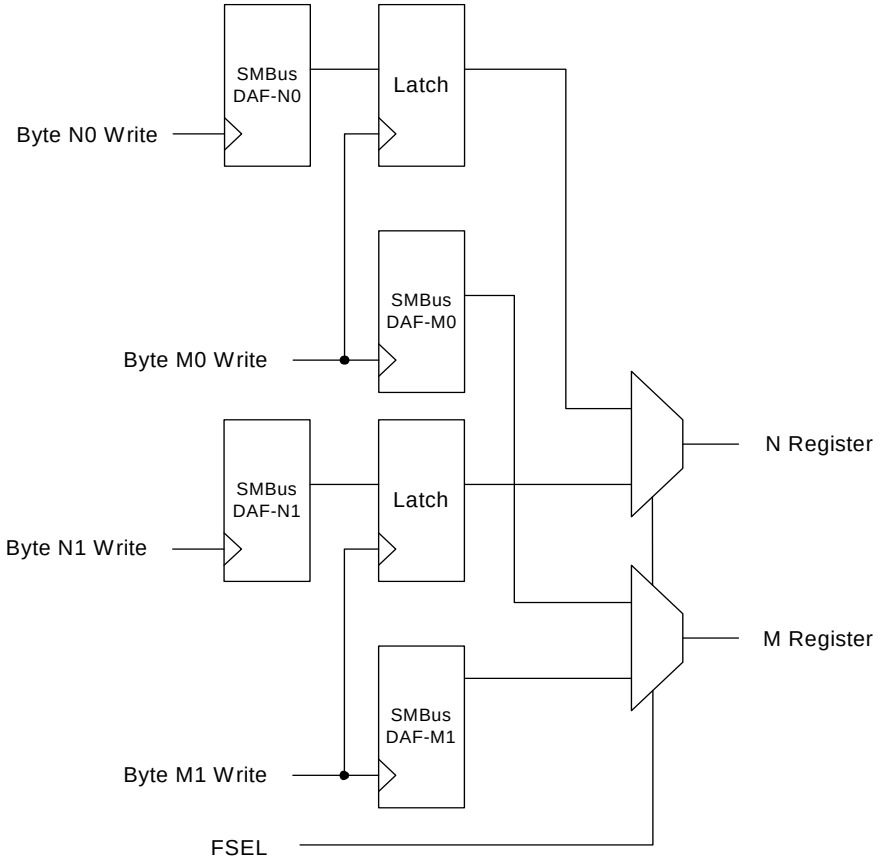



**Figure 1. Dial-a-Frequency Register Switching and Synchronizer Circuitry**

This circuitry is designed to present simultaneous M&N values to the VCO when writing to the $I^2C$ lines. If not for this delay in writing the N register value, the VCO would use a new N value and an old M value and would go to an indeterminate frequency until the next $I^2C$ byte was written.

## Crystal Recommendations

The CY28508 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28508 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

## Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL). *Figure 2* shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal.

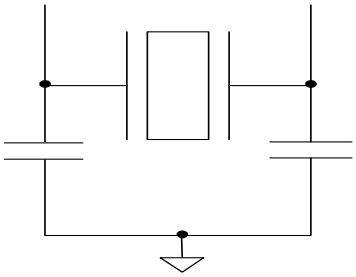


**Figure 2. Crystal Capacitive Clarification**

**Table 5. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|---|---|---|---|---|---|---|---|---|---|
| 14.31818 MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 50 ppm | 50 ppm | 5 ppm |

## Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

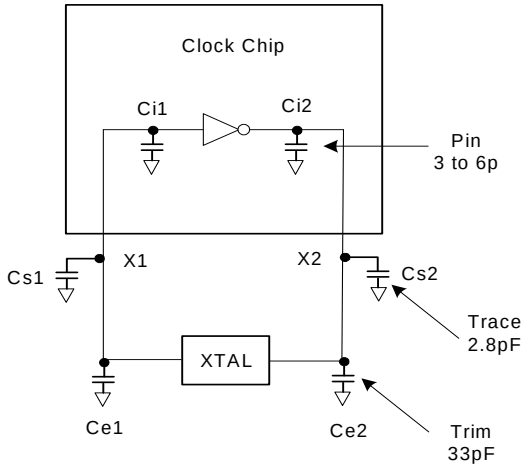



**Figure 3. Crystal Loading Example**

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1, Ce2) should be calculated to provide equal capacitive loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

**Load Capacitance (each side)**

$$Ce = 2 * CL - (Cs + Ci)$$

**Total Capacitance (as seen by the crystal)**

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL.....Crystal load capacitance

CLe..... Actual loading seen by crystal using standard value trim capacitors

Ce..... External trim capacitors

Cs..... Stray capacitance (trace, etc.)

Ci ..... Internal capacitance (lead frame, bond wires, etc.)

### CPU_STOP# Clarification

The CPU_STOP# signal is an active LOW input used for synchronous stopping and starting of the CPU output clocks while the rest of the clock generator continues to function. The REF output is not affected by the CPU_STOP# signal.

### CPU_STOP# Assertion

When CPU_STOP# pin is asserted, all CPUT/C outputs will be stopped after being sampled by two rising edges of the CPUT clocks. The final state of the stopped CPU signals is CPUT = LOW and CPU0C = HIGH.

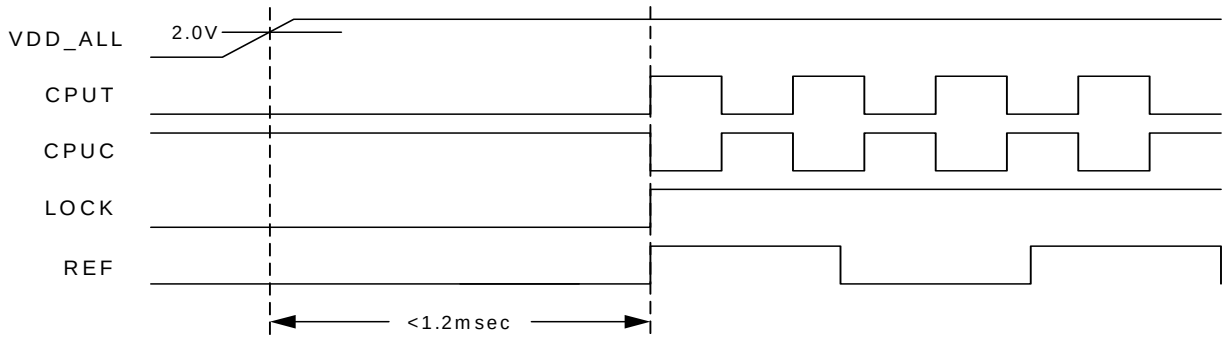



**Figure 4. Power-up Signal Timing**

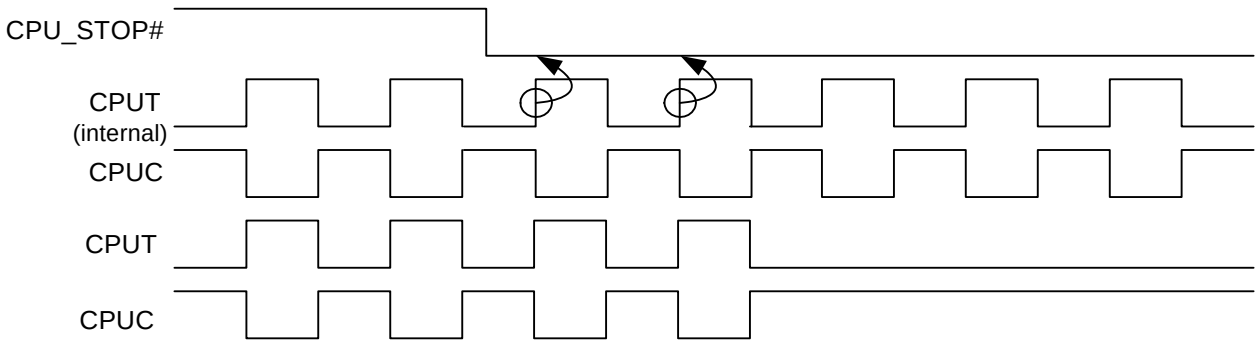



**Figure 5. CPU_STOP# Assertion Waveform**

**CPU_STOP# Deassertion**

The deassertion of the CPU_STOP# signal will cause all CPUT/C outputs that were stopped to resume normal operation in a synchronous manner. Synchronous manner meaning that no short or stretched clock pulses will be produces when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPUC clock cycles.

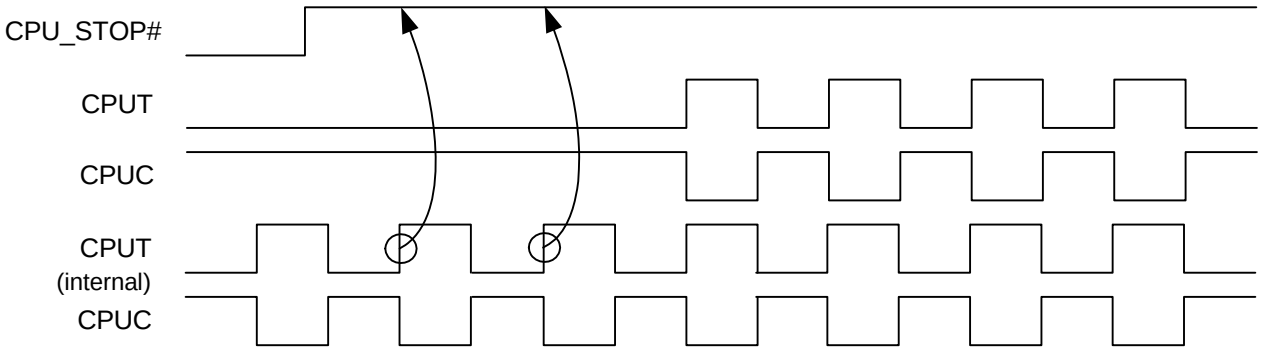



**Figure 6. CPU_STOP# Deassertion Waveform**

## Absolute Maximum Conditions[2]

| Parameter | Description | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDC}$, $V_{DDA}$, $V_{DDX}$ | 3.3V Supply Voltage | Maximum functional voltage | –0.5 | 5.5 | V |
| $V_{DDQ}$ | Analog Supply Voltage | Maximum functional voltage | –0.5 | 5.5 | V |
| $V_{IN}$ | Input Voltage | Relative to $V_{SS}$ | –0.5 | $V_{DD}$ + 0.5 | V |
| $T_S$ | Temperature, Storage | Non-functional | –65 | 150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | 0 | 70 | °C |
| $T_J$ | Temperature, Junction | Functional | | 150 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | – | V |
| $Ø_{JC}$ | Dissipation, Junction to Case | Mil-Spec 883E Method 1012.1 | 42 | | °C/W |
| $Ø_{JA}$ | Dissipation, Junction to Ambient | JEDEC (JESD 51) | 118 | | °C/W |
| UL–94 | Flammability Rating | At 1/8 in. | V–0 | | |
| MSL | Moisture Sensitivity Level | | 1 | | |

## DC Electrical Specifications

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDA}$, $V_{DDX}$, $V_{DDC}$ | 3.3 Operating Voltage | 3.3 ± 5% | 3.135 | 3.300 | 3.465 | V |
| $V_{DDQ}$ | 2.5 Operating Voltage | 2.5 ± 5% | 2.375 | 2.500 | 2.625 | V |
| $V_{IL}$ | Input Low Voltage | $V_{IL}$ for all inputs except XIN | | | 1.0 | Vdc |
| $V_{IH}$ | Input High Voltage | $V_{IH}$ for all inputs except XIN | 2.0 | | | Vdc |
| $I_{ILC}$ | Input Leakage Current | Except for internal pull-up or pull-down resistors | –5 | | 5 | µA |
| $I_{IL}$ | Input Low Current (@VIL = VSS) | For internal pull-up resistors | 9 | | | µA |
| $I_{IH}$ | Input High Current (@VIL =VDD) | For internal pull-down resistors | –9 | | | µA |
| $I_{OLI2C}$ | $I^2C$ Sink Current | | | | | mA |
| $V_{OL}$ | Output Low Voltage | REF output | | | 0.4 | Vdc |
| $V_{OH}$ | Output High Voltage | REF output | 2.4 | | | Vdc |
| $V_{OLC}$ | Output Low Voltage CPU | At load measurement point with recommended termination. See *Figure 7*. | 0.0 | | 0.4 | Vdc |
| $V_{OHC}$ | Output High Voltage CPU | At load measurement point with recommended termination. See *Figure 7*. | 0.6 | | 1.6 | Vdc |
| $V_{XIH}$ | Xin High Voltage | | $0.7V_{DDX}$ | | $V_{DDX}$ | V |
| $V_{XIL}$ | Xin Low Voltage | | 0 | | $0.3V_{DDX}$ | V |
| $I_{OZ}$ | Three-state leakage Current | | | | 10 | µA |
| $C_{IN}$ | Input Pin Capacitance | For all pins including XIN | | | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | | | 6 | pF |
| $L_{IN}$ | Input Pin Inductance | | | | 7 | nH |
| $Z_{OUT}$ | Output Impedance of CPU Clock | Both rising and falling | | 18 | | Ω |
| $I_{DD3A}$ | Power supply current for all 3.3V VDDs with all three buffers enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 80 | 100 | mA |
| $I_{DD3B}$ | Power supply current for all 3.3V VDDs with VDDs with two buffers enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 78 | 100 | mA |
| $I_{DD3C}$ | Power supply current for all 3.3V VDDs with one buffer enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 77 | 100 | mA |

**Note:**
2. Multiple Sequence: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## DC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{DDR}$ | Power supply additional current for all 3.3V VDDs for loaded REF only | Output is 14.31818 MHz with VCO running 666.6 MHz | | 8 | 10 | mA |
| $I_{DD2A}$ | Power supply current for all 2.5V VDDs with three buffers enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 180 | 225 | mA |
| $I_{DD2B}$ | Power supply current for all 2.5V VDDs with two buffers enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 124 | 155 | mA |
| $I_{DD2C}$ | Power supply current for all 2.5V VDDs with one buffer enabled and loaded | Output is 224.7 MHz with VCO running 666.6 MHz | | 70 | 90 | mA |
| $I_{DD2D}$ | Power supply current for all 2.5V VDDs with all buffers disabled | Output is 224.7 MHz with VCO running 666.6 MHz | | 7 | 10 | mA |

## AC Electrical Specifications

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Crystal** | | | | | | |
| $T_{DC}$ | Xin Duty Cycle | Measured at $V_{DDX}/2$ | 45 | | 55 | % |
| $T_{PERIOD}$ | Xin Period | Measured at $V_{DDX}/2$. The VCO frequency must remain within its operating range. | 52.4 | 69.841 | 87.3 | ns |
| **REF Output** | | | | | | |
| $T_{DC}$ | REF Duty Cycle | Measured at 1.5V, 15-pF lumped load. | 45 | 50 | 55 | % |
| $T_{RISE}/T_{FALL}$ | REF Rise and Fall Times | Measured from 0.4V to 2.4V, 15-pF lumped load. | 1 | | 4 | ns |
| $T_{CCJ}$ | REF Cycle to Cycle Jitter | Measured at 1.5V, 15-pF lumped load. | | | 1000 | ps |
| **LOCK Output** | | | | | | |
| $T_{FALL}$ | Lock Fall Time | Measured from 2.4V to 0.4V, 10-pF lumped load and 10KΩ pull-up. | 0.5 | | 2 | ns |
| **CPU Outputs** | | | | | | |
| $T_{DC}$ | CPUT/C Duty Cycle | Measured at 0.62V at measuring point. See *Figure 7.* | 45 | 50 | 55 | % |
| $T_{RISE}/T_{FALL}$ | CPUT/C Rise and Fall Times | Measured from 0.3V to 0.9V. See *Figure 7.* | 150 | | 500 | ps |
| $T_{SKEW}$ | CPUT/C to CPUT/C Clock Skew | Measured at 0.62V at measuring point. See *Figure 7.* | | | 100 | ps |
| $T_{CCJ}$ | CPUT/C Cycle to Cycle Jitter | Measured at 0.62V at measuring point. See *Figure 7.* | | | 135 | ps |
| $V_{DIF}$ | Differential Voltage Swing | At load measuring point. See *Figures 7 and 8.* | | 1.24 | 1.5 | |
| $V_{OX}$ | Crossing Point Voltage | At load measuring point. See *Figures 7 and 8.* | 0.4 | 0.62 | 0.9 | V |
| $F_{VCO}$ | VCO Operating Frequency | Over voltage, temperature and process | 333 | | 675 | MHz |
| $T_{XS}$ | Power-on Hold Off | Outputs will be as shown in *Figure 6* | | | 1.2 | ms |

**Table 6. Slew Rate Settings Output Divider = /3 (Measured over 10 μs)**

| M | N Range | Typ. Max. Slew Rate (kHz/μS) | Worst-Corner Max Slew Rate (kHz/μS) | ICP B2b7 | Ns B7b7 | Variable ICP B8b7 |
|---|---|---|---|---|---|---|
| 49 | 43-65 | 55 | 100 | x1 | 2048 | 1 |
| 49 | 65-86 | 75 | 140 | x1 | 2048 or 1024 | 1 |
| 49 | 43-86 | 45 | 70 | x1 | 2048 | 0 |

**Table 7. Slew Rate Settings Output Divider = /2 (Measured over 10 μs)**

| M | N Range | Typ. Max. Slew Rate (kHz/μS) | Worst-Corner Max Slew Rate (kHz/μS) | ICP B2b7 | Ns B7b7 | Variable ICP B8b7 |
|---|---|---|---|---|---|---|
| 49 | 43-65 | 80 | 150 | x1 | 2048 | 1 |
| 49 | 65-86 | 120 | 200 | x1 | 2048 or 1024 | 1 |
| 49 | 43-86 | 65 | 100 | x1 | 2048 | 0 |

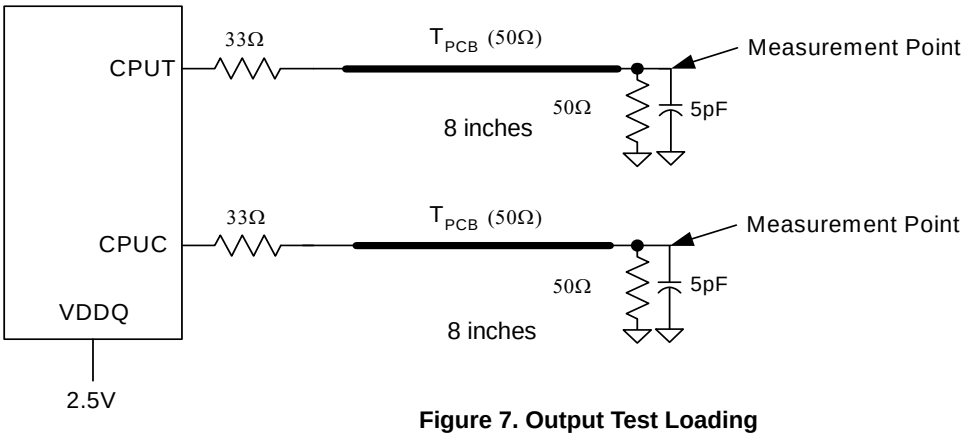



**Figure 7. Output Test Loading**

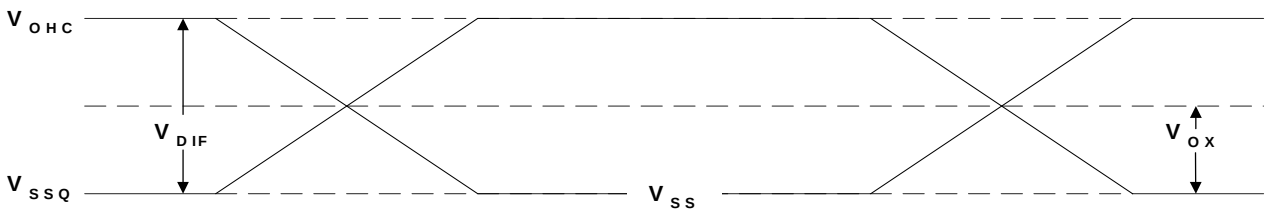


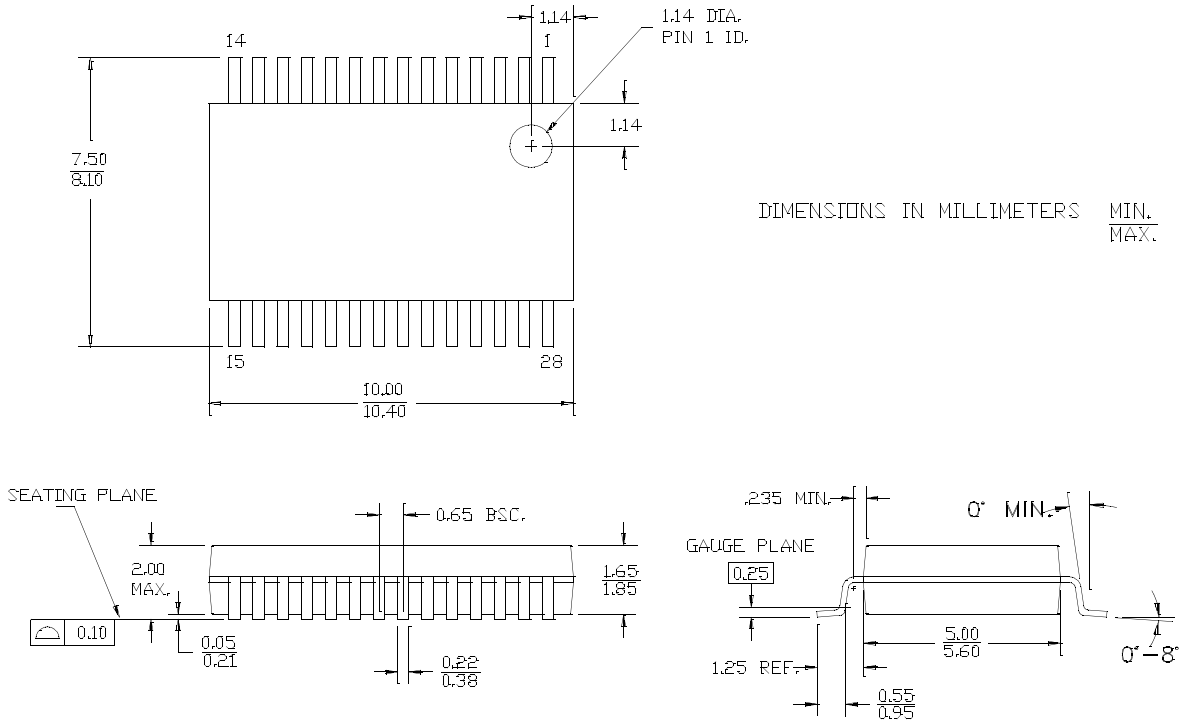

**Figure 8. CPU Signaling**

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY28508OC | 28-pin SSOP | Commercial, 0° to 70°C |
| CY28508OCT | 28-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |
| **Lead- Free** | | |
| CY28508OXC | 28-pin SSOP | Commercial, 0° to 70°C |
| CY28508OCXT | 28-pin SSOP – Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

**28-lead (5.3 mm) Shrunk Small Outline Package O28**



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